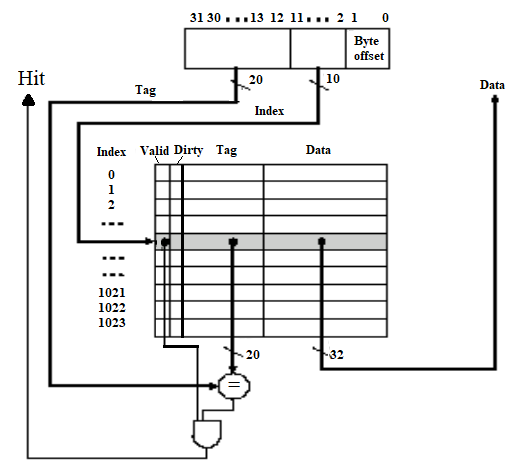
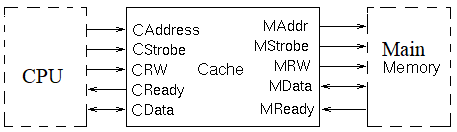
The architecture of a direct mapped cache required in this project is shown below:



Design the direct mapped cache module which can interface with CPU and Main Memory shown below:



The direct mapped cache uses write back with write allocation policy.

CAddress: cache address

CStrobe: high active cache strobe

CRW: Cache read/write. 1: read; 0: write

CReady: high active Cache ready

CData: data bus between Cache and CPU

MAddr: main memory address

MStrobe: high active main memory strobe

MData: data bus between Cache and main memory

Mready: high active Main Memory ready

MRW: Main memory read/write. 1: read; 0: write